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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/761,322

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Akihiko Hirano

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EXAMINER

FIGUEROA, NATALIA

ART UNIT

PAPER NUMBER

2651

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/761,322

Applicant(s)

HIRANO ET AL.

Examiner

Natalia Figueroa

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-16 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4,5,9,12 and 14-16 is/are allowed.
- 6) ☒ Claim(s) 2,6,10,11 and 13 is/are rejected.
- 7) ☐ Claim(s) 3,7 and 8 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 01/22/2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

1. This Office Action will replace all previous Office Action, and the time period will be reinstated to reflect the mailing date this Office Action. Examiner is providing the non-patent documents cited in Form PTO-892.
2. Preliminary amendment submitted by the applicant filed on 27 January 2004 has been received and considered by the examiner.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), which papers have been placed of record on file

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 22 January 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

5. Claims 4, 10, 13, 14 and 15 are objected to because of the following informalities:

RE claim 4, the language (according to claim 3) is improper. The actual limitations of claim 3 should be inserted in its place.

RE claims 10 and 14, the language (according to claim 8) is improper. The actual limitations of claim 8 should be inserted in its place.

RE claim 13, the language (according to claim 11) is improper. The actual limitations of claim 11 should be inserted in its place.

RE claim 15, the language (according to claim 12) is improper. The actual limitations of claim 12 should be inserted in its place. Appropriate correction is required in all of the above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by “Correction Methods for Errors in Partial Response Channels”, hereinafter NN70031724.

RE claim 2, NN70031724 discloses a record signal processing circuit comprising a coding device for inputting data to be recorded and coding the input data into a bit stream of a coded word with a parity (page 1, ¶ 1-2); and a precoder for inputting an output of said coding device, and performing precoding according to $1/(1+D)$ as a delay operator (page 1, ¶ 2-3), wherein said coding device calculates a parity bit with a pattern corresponding to an output of said precoder before the precoding, and performs bit conversion with a bit stream containing the parity bit (page 1, ¶ 3-4), and wherein said precoder outputs data to be recorded as a bit stream of a coded word with a coded parity (page 1, ¶ 3-4).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over NN70031724 in view of Aziz et al (USPN 6,130,329), hereinafter Aziz.

RE claim 6, NN70031724 discloses generating a parity bit for error detection, and adding the parity bit to the bit stream of the coded word (page 1, ¶ 3-4); a parity generating circuit for inputting the bit stream of the coded word from said coding device (page 1, ¶ 1-3); a precoder for inputting an output of said parity generating circuit, and performing precoding according to $1/(1+D)$ as a delay operator (page 1, ¶ 1-3); and wherein said recording is performed in such a manner that a value of a parity bit resulting from parity calculation of a bit stream as a target of the parity bit among bit streams recorded on said information recording medium does not necessarily coincide with a value of a parity bit recorded on said Information recording medium correspondingly to the bit stream recorded on said information recording medium (page 1, ¶ 3-5).

NN70031724 fails to explicitly teach an information recording apparatus comprising a coding device for inputting data to be recorded and coding the input data into a bit stream of a coded word; an information recording medium for recording data; and a recording head for recording data on said information recording medium, wherein said recording head records data

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on said information recording head according to the bit stream of the coded word outputted from said precoder. However, Aziz discloses such information recording apparatus and medium in (fig. 1, col. 1, lines 19-44 and col. 4, lines 1-24, Aziz inherently teaches an interface circuit and controller because these elements are contained in all disk drive systems).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method as disclosed by NN70031724 with the above teachings from Aziz the motivation being to therefore eliminate the most common error associated with partial response maximum likelihood, hence avoiding the corruption or loss of data.

11. Claims 10, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aziz in view of Nikolic et al (USPN 6,081,210), hereinafter Nikolic.

RE claim 10, Aziz discloses an information reproducing apparatus comprising an information recording medium for recording data; a reproducing head for reproducing data recorded on said information recording medium, wherein said reproducing head obtains a reproduction signal from said information recording medium, and said information reproducing circuit inputs the reproduction signal, and outputs reproduced data (fig. 1, col. 1, lines 19-44 and col. 4, lines 1-24, Aziz inherently teaches an interface circuit and controller because these elements are contained in all disk drive systems). Aziz fails to explicitly teach a reproduction signal processing circuit according to claim 8. However, Nikolic discloses such on (see abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method as disclosed by Aziz with the above teachings

from Nikolic the motivation being to therefore eliminate the most common error associated with partial response maximum likelihood as set forth in the abstract.

RE claim 11, the combination of Aziz and Nikolic is relied upon for the same reasons of rejection as stated above. Nikolic further discloses that the data recorded on said information recording medium has a continuous number "r" not larger than 3 or 4 of reverse times of record state or recorded information (see abstract).

RE claim 13, Aziz discloses an information recording and reproducing apparatus comprising an information recording medium for recording data and a recording/reproducing head for recording/reproducing data on/from said information recording medium (fig. 1, col. 1, lines 19-44 and col. 4, lines 1-24, Aziz inherently teaches an interface circuit and controller because these elements are contained in all disk drive systems). Aziz fails to explicitly teach an information recording and reproducing circuit according to claim 11, wherein the data recorded on said information recording medium has a continuous number "r" not larger than 3 or 4 of reverse times of record state of recorded information. However, Nikolic discloses such on (see abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method as disclosed by Aziz with the above teachings from Nikolic the motivation being to therefore eliminate the most common error associated with partial response maximum likelihood as set forth in the abstract.

Allowable Subject Matter

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12. Claims 3, 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record, and in particular "Correction Methods for Errors in Partial Response Channels", fails to teach or suggest a record signal processing circuit that, when performing the bit conversion with the bit stream containing the parity bit, said coding device performs either conversion of bit patterns "*01-1-110", "011-1-10*" and "011-1-110" (* is don't care) with the parity bit being "0", or conversion of a bit pattern "011-1-10" with the parity being "0", where a bit stream of a coded word of 3 bits immediately before the parity bit, one bit of the parity bit, and a bit stream of a coded word of 3 bits immediately after the parity bit are separated by a symbol"-".

14. Claims 4-5, 9, 12, 14-15 and 16 are allowed.

15. The following is an examiner's statement of reasons for allowance:

RE claim 4, the prior art of record, and in particular "Correction Methods for Errors in Partial Response Channels", fails to teach or suggest an apparatus comprising a record signal processing circuit according to claim 3.

Re claims 9 and 12, the prior art of record, and in particular "Correction Methods for Errors in Partial Response Channels", fails to teach or suggest a Viterbi decoding circuit performs data discrimination by excluding from search candidates a transition path corresponding to a coded word series "1111" in a process of searching a most likelihood path corresponding to a case where the l's continuous number "r" is 3, or by excluding from search

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candidates a transition path corresponding to a coded word series "1111" in a process of searching a most likelihood path corresponding to a case where the l's continuous number "r" is 4, or by excluding from search candidates transition path: corresponding to coded word series "1111", "001111" and "111100", in a process of searching a most likelihood path corresponding to a case where the l's continuous number "r" is 4; and said decoder includes a bit reverse-converting circuit and an error correction circuit, in which said bit reverse-converting circuit performs reverse-conversion of discriminated bit stream in a case of a bit stream of either "****-0-1110" or "0111-0-****" (* is don't care), where a bit stream of a coded word of 4 bits immediately before the parity bit, one bit of the parity bit, and a bit stream of a coded word of 4 bits immediately after the parity bit are separated by a symbol "-", and said error correction circuit corrects discrimination errors of 1 bit and 3 bits.

Re claim 14, the prior art of record, and in particular "Correction Methods for Errors in Partial Response Channels", fails to teach or suggest an apparatus comprising an information recording apparatus including that when performing the bit conversion with the bit stream containing the parity bit, said coding device performs either conversion of bit patterns "*01-1-110", "011-1-10*" and "011-1-110" (* is don't care) with the parity bit being "0", or conversion of a bit pattern "011-1-10" with the parity being "0", where a bit stream of a coded word of 3 bits immediately before the parity bit, one bit of the parity bit, and a bit stream of a coded word of 3 bits immediately after the parity bit are separated by a symbol "-".

Re claim 15, the prior art of record, and in particular "Correction Methods for Errors in

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Partial Response Channels”, fails to teach or suggest an apparatus comprising an information recording and reproducing circuit according to claim 12 for performing signal processing of data outputted from said hard disk controller.

16. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents are cited to further show the state of the art with respect to decoding apparatus.

a) Fitzpatrick et al (USPN 5,949,357): Discloses an encoding/decoding apparatus.

b) T. Conway (*A New Target Response ...*): Discloses parity coding for magnetic recording channels.

c) McClellan (USPN 6,243,847): Discloses a PRML read channel.

d) McClellan (USPN 6,282,690): Discloses a parity insertion method.


18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Natalia Figueroa whose telephone number is (571) 272-7554. The examiner can normally be reached on Monday - Thursday 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David R. Hudspeth can be reached on (571) 272-7843. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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